



PATENT ABSTRACTS OF JAPAN

(11) Publication number: **10214062 A**(43) Date of publication of application: **11.08.98**

(51) Int. Cl.

G09G 3/36
G02F 1/133
G02F 1/133

(21) Application number: **09015187**(22) Date of filing: **29.01.97**(71) Applicant: **HOSHIDEN PHILIPS DISPLAY KK**

(72) Inventor: **KAMIYA OSAO**
WATANABE HIDETOSHI

(54) **LIQUID CRYSTAL DISPLAY ERASING CIRCUIT
 FOR POWER-OFF TIME**

COPYRIGHT: (C)1998,JPO

(57) Abstract:

PROBLEM TO BE SOLVED: To erase a liquid crystal display even at power-OFF time even unless a shift register in a gate bus driving circuit has a reset function.

SOLUTION: A power source holding circuit 10 holds the electric power of an operating power source supplied to the gate bus driving circuit for a specific time even after the power source is turned off and supplies source voltages V1b and V2b ($V1b > V2b$) to the gate bus driving circuit 7. When a shift pulse generator 23 and an H-level voltage generator 24 are supplied with the operating electric power from the power source holding circuit 10 and the output of a voltage drop detecting circuit 14, the former supplies a shift pulse SP to a shift register 8 and the latter supplies data Vout of H level corresponding to logic '1'. Consequently, the operation of the gate bus driving circuit 7 is held for the specific time even after the power source is turned off and during a prescribed period, FETs of respective pixels are turned on to discharge accumulated electric charges.

